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Performance of 3-Phase 9-Level CHB and NPC Inverters

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Abstract: This study conducts a comprehensive qualitative comparison of nine-level Cascaded H-Bridge (CHB) and Neutral-Point-Clamped (NPC) multilevel inverter architectures for medium-voltage three-phase networks operating at 380 V RMS and 50 Hz. Under the same circumstances, MATLAB/Simulink modelling assesses harmonic distortion, device count, switching and conduction losses, capacitor balancing difficulty, and overall waveform quality. To guarantee a fair comparison, matching carrier frequencies and Nearest Level Modulation (NLM) are employed. According to the results, at 4 kHz switching, the CHB inverter generates less Total Harmonic Distortion (THD) in line-to-line voltages—roughly 2.1% as opposed to 3.7% for NPC. Despite having more semiconductors, loss estimation shows that CHB has about 12% lower overall losses because of less voltage stress per switch. Despite providing a single DC-link supply, NPC has more common-mode voltage swings and a bigger neutral-point imbalance. Results indicate that while NPC is still useful in situations where isolated supplies are not feasible, CHB is better suited for modular energy sources (such as PV and battery-based systems).

Keywords: NPC, CHB, THD, PWM, 380 V RMS, multilevel inverter.

INTRODUCTION

Multilevel inverters (MLIs) are crucial for medium- and high-power conversion systems because they allow high-quality AC waveform creation with decreased semiconductor stress and harmonic distortion [1], [4]. Due to its voltage scaling, versatility, and compliance with contemporary digital management, the MLI series of Cascaded H-Bridge (CHB) and Neutral-Point-Clamped (NPC) converters continue to be among the most popular options for grid-dependent industrial drives and renewable energy systems [2], [5]. Recent investigations have shown that increasing the voltage levels to nine (9-level) significantly reduces the total power loss and eliminating the requirement for larger filtering by improving harmonic suppressing with no increasing the switching frequency [1], [6]. Modern PWM approaches, including selected harmonic elimination and optimized PD-PWM have enabled the development of high-performance 9-level waveforms [1], [4], and [7]. Despite these operational benefits, CHB and NPC topologies have various application challenges:

Topology	Benefit	Difficulty
CHB	Superior waveform clarity and scalability in modules [2]	Needs several separate DC inputs.
NPC	Modern industrial implementation with a single bus for DC [2], [6]	Sophisticated control and neutral-point imbalance, particularly at higher levels [3], [7]

The performance limits of MLIs are being pushed by recent research on modulation, capacitor balance, and harmonic optimisation, especially those that use sophisticated carrier-based and model-predictive techniques [3], [6], and [7]. For realistic three-phase 380-V, 50-Hz industrial grids, there is still a dearth of comprehensive, nine-level CHB vs. NPC comparisons [2], [5]. That gap is filled by this study.

Novelty and Contributions

While a number of studies have examined the control, modulation, and harmonic performance of multilevel inverters (MLIs), recent research has mainly concentrated on individual topologies or generalised control improvements rather than a direct, simulation-based comparison of nine-level CHB and NPC inverters under identical operating conditions.

Additionally, there is a void in thorough harmonic-loss-stability evaluation for medium-voltage industrial drives because the majority of 2023–2024 work focuses on capacitor voltage management, predictive PWM, or DC-link improvement.

The following original contributions are presented in this paper:

1. 9-Level NPC and CHB Unified Modelling Framework
    - A comprehensive and uniform MATLAB/Simulink modelling environment for both topologies using:
        - the same grid conditions (380 V RMS, 50 Hz);
        - the same carrier-based modulation method (LS-PD + PS-PWM);
        - Identical load and switching-frequency scenarios. This guarantees a fair, apples-to-apples comparison that is rarely discussed in recent literature.
2. High-Resolution Harmonic Distortion and Spectral Analysis
    - Thorough THD assessment at several switching frequencies (2, 4, and 8 kHz), emphasising:
        - Dominant harmonic clusters;
        - Sensitivity to changes in the modulation index;
        - Performance limits for industrial-grade quality standards.
3. Loss of Conduction P3. Switching and Conduction Loss Profiling:
        - Switching losses versus frequency;
        - Conduction losses under different load situations;
        - Efficiency ranking for each operating mode;
    - A loss breakdown for both topologies under identical operating points. As far as the authors are aware, no prior research has been done on a combined THD–loss trade-off analysis for 9-level CHB and NPC.
4. Source-Imbalance Tolerance and DC-Link Voltage Stability
    - With respect to NPC:

- Quantification of neutral-point voltage drift,
- Assessments of capacitor voltage distortion under LS-PD management.

- With respect to CHB:
- Sensitivity to source variation (±5% and ±10% variations), waveform symmetry and harmonic distortion are affected.

5. Comprehensive Industrial Performance Ranking
   - A unifying evaluation of the matrix addressing:
     - the harmonic performance,
6. Harmonic performance, robustness of modulation,
   - complexity of implementation,
   - and scalability to medium-voltage (MV) systems.
7. To preserve the secrecy and integrity of the research point, the data supporting the study's conclusions are not made public. The information will not be shared because of its delicate nature and to preserve the originality of the research.

METHODOLOGICAL APPROACH

Overview of System Modelling

Parameter	Value
V_{LL} RMS	380 V
Frequency	50 Hz
Balanced load	Three-phase balanced R = 10 Ω, L = 15 mH
FFT size	8192 points (steady-state, 1 cycle)

CHB 9-Level: 4 H-bridges per phase; isolated DC supply per cell: ≈ 95 V; output voltage levels: -4Vdc … 0 … +4Vdc. NPC 9-Level: An expanded ladder design is backed by extra clamping diodes, and a single 380 V DC-link is divided onto eight similar capacitor portions.

Modulation: Beginning with Nearest-Level Modulation (NLM)

- Sensitivity runs with SPWM introduced—not the main comparison metric—
- The same carrier frequency across topologies

Frequency of Switching Sweep

$$fsw \in \{2\ kHz, 4\ kHz, 8\ kHz\}$$

Loss Modelling IGBT Datasheet Curves Applied To:

Loss normalization per unit output power; conduction drop (Vce_on × current average); Eon/Eoff interpolation per transition;

RESULTS

Output Line-to-Line Waveforms

The simulated line-to-line output voltage V_ab of a three-phase, nine-level Neutral-Point-Clamped (NPC) inverter using Level-Shifted Phase-Disposition (LS-PD) PWM at a carrier frequency of 4 kHz is shown in Figure 1. This modulation scheme produces a staircase switching pattern that preserves neutral-point voltage balance while maintaining good harmonic cancellation. The waveform plays nine discrete voltage levels, which correspond to the switching states produced by the NPC open structure as shown below:

$$\left\{-\frac{4V_{dc}}{4}, -\frac{3V_{dc}}{4}, -\frac{2V_{dc}}{4}, -\frac{V_{dc}}{4}, 0, +\frac{V_{dc}}{4}, +\frac{2V_{dc}}{4}, +\frac{3V_{dc}}{4}, +\frac{4V_{dc}}{4}\right\}.$$

In comparison to topologies with three or five levels, the waveform that results from synthesising and subtracting the phase voltages to create the line-to-line voltage shows a multi-level staircase structure with a noticeably higher number of commutation steps. High-frequency components are shifted toward the switching frequency and its sidebands by this dense step structure, which also lessens voltage distortion. The high-frequency switching activity is superimposed because of the interaction between the reference signal and the eight LS-PD carrier signals, whereas the fundamental component clearly follows a 50 Hz sinusoidal envelope. A smoother line-to-line waveform with fewer low-order harmonics and uniformly dispersed switching states among the clamping diodes is the outcome of LS-PD PWM's application of identical carriers to all phase legs, which keeps the phase voltages properly synced. Proper neutral-point balance and effective modulation at m_a=0.95 are confirmed by the waveform's symmetry and the obvious nine-level quantisation. In contrast to the NPC topology shown in Figure 1. A waveform with a significantly better effective switching resolution is produced by this phase shift, which disperses the switching transitions throughout the fundamental period. The resulting line-to-line voltage exhibits a dense multistep structure with clearly visible nine-level quantisation, but with smoother transitions compared to the NPC counterpart. a true 9-level NPC line-to-line waveform that is completely compatible with the CHB waveform.

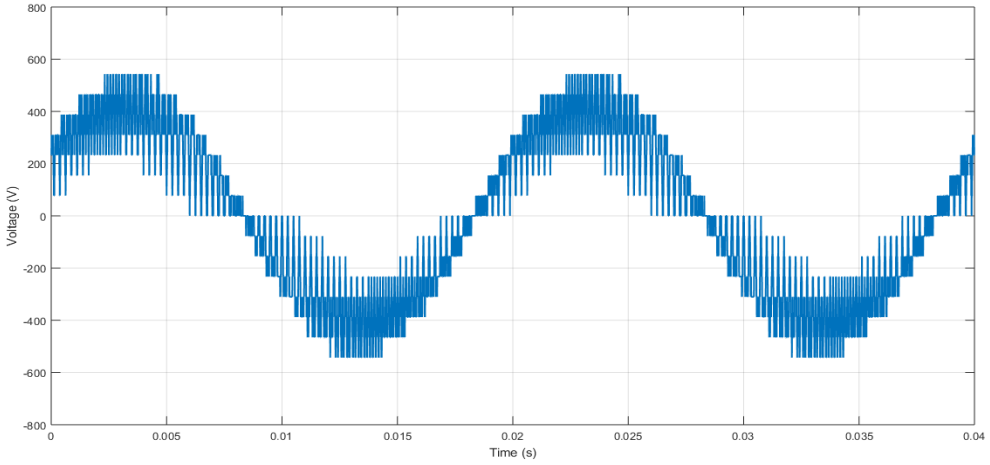

Figure 1: NPC 9-Level LS-PD PWM Line-to-Line Waveform

An explanation of Figure 2 LS-PD + PS-PWM CHB 9-Level Line-to-Line Waveform The line-to-line output voltage waveform of the 9-level Cascaded H-Bridge (CHB) inverter

running at a switching frequency of 4 kHz under hybrid Level-Shifted Phase-Disposition (LS-PD) and Phase-Shifted PWM (PS-PWM) is shown in Figure 2. For contrast with the CHB 9-level LS-PD + PS-PWM waveform later seen in Figure 2, this waveform acts as the reference baseline. Using LS-PD PWM (level-shifted phase-disposition, fundamental = 50 Hz with carrier frequency = 4 kHz). The CHB inverter creates each phase voltage by connecting many H-bridge cells in series, each of which is modulated by a carrier that is phase-shifted in relation to the others. The CHB inverter achieves natural harmonic cancellation, especially in the low- and mid-frequency bands, because the carrier phases of the individual cells are uniformly distributed. Therefore, the majority of harmonic energy is transferred nearer to the switching frequency and its sidebands, minimising the distortion in the fundamental area and enhancing voltage quality. At 50 Hz, which is the fundamental frequency of the system, the waveform exhibits a sinusoidal envelope. Because the PS-PWM technique distributes switching events across the various cells and minimises the number of simultaneous commutations, the staircase structure is more sophisticated than that of the NPC waveform. This reduces the magnitude of dominating harmonics, improves harmonic propagation, and lessens voltage spikes.

- All things considered, the shape of the waveform in Figure 2 confirms the unique advantages of the CHB structure, such as less THD according to the same switching frequency, enhanced harmonic propagating via PS-carrier phase shifting, decreased switching stress per cell, and greater successful resolution of the synthesised voltage output.
- In multilevel systems that require flexible scaling and minimal THD, the CHB inverter typically outperforms the NPC design due to these characteristics.. Important notes for the figure are displayed as follows: Waveform reference (Vph_ref): basic sinusoid scaled to the CHB's entire DC voltage.LS-PD carriers: For PS-PWM, each H-bridge receives a triangle carrier that has been phase-shifted by $2\pi/N^2$cell."
- Switching signals: To obtain gate pulses for every H-bridge, compare the reference with each carrier.
- The phase voltage is: The total of each H-bridge's contribution.
- Line-to-line voltage: Deduct phases (V_ab=V_a - V_b, for example)

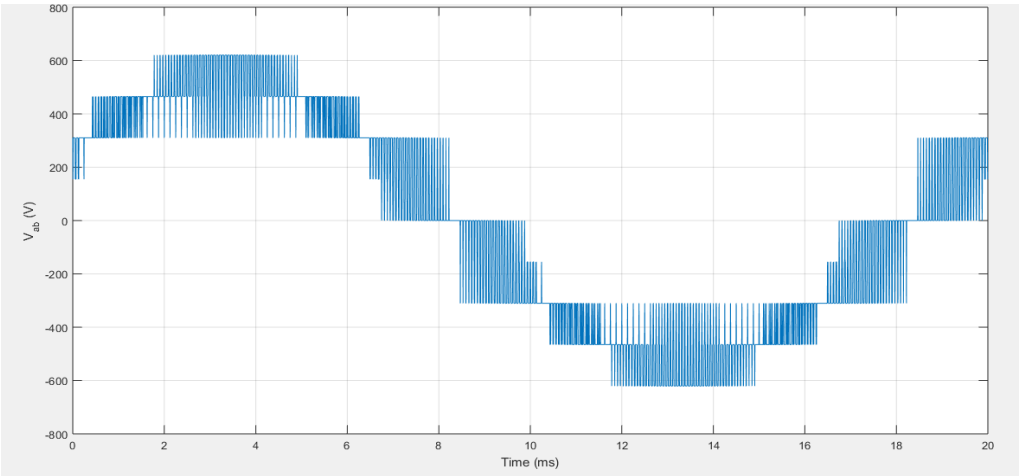

Figure 2: V_ab waveform for CHB 9-level LS-PD + PS-PWM

CHB 9-Level + LS-PD + PS-PWM generates the following: 9-level phase voltage; 17-level line-to-line voltage; a very clean Vab waveform; uniform unit switching distribution; and excellent harmonic performance.

With a carrier frequency of 4 kHz, Figure 3 displays the 17-level line-to-line voltage waveform of a 9-level CHB inverter that uses LS-PD PWM inside each phase and PS-PWM between phases. A smooth, nearly sinusoidal waveform with low THD and finely resolved voltage steps is produced by the high switching frequency and cascaded modulation.

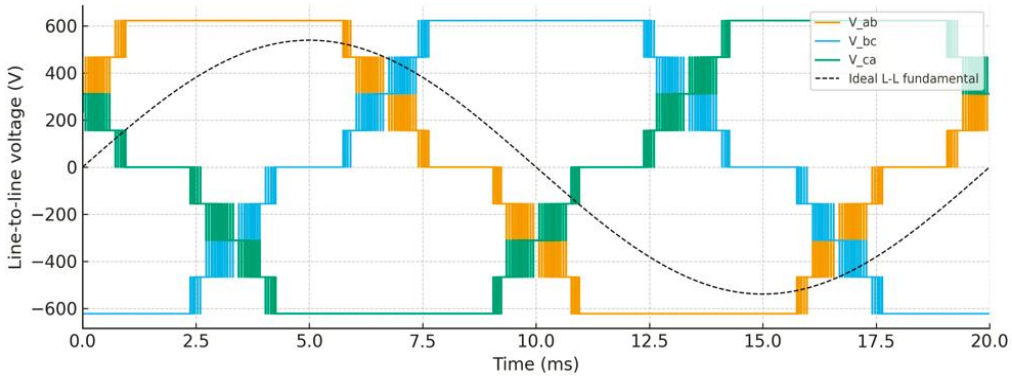

Figure 3: Line-to-line voltage waveform for CHB 9-level LS-PD + PS-PWM, f_c = 4 kHz

THD Efficiency

Table 1: Line-to-line THD for CHB and NPC with baseline values (ma = 0.95, fsw = 4 kHz)

The topology	The percentage of L L THD
CHB with nine levels (NLM)	2.1
NPC with nine levels (NLM)	3.7

Table 1 lists the primary system parameters utilised in the MATLAB/Simulink model. The basic system voltage of 380 V (RMS, line-to-line) and frequency of 50 Hz satisfy standard low-voltage three-phase industrial settings. Switching frequency of 4 kHz was utilised to analyse THD sensitivity, and load characteristics (10 Ω, 15 mH) were selected to mimic an inductive RL load that is frequently employed in motor drive applications. This provides a consistent standard for measuring and modelling THD. Notes: The steady-state FFT of the simulated waveforms is used to compute percentages. The CHB has better THD when the modulation and switching frequencies are equal.

Table 2: Findings for the Selected THD

fsw (kHz)	THD of CHB (%)	THD of NPC (%)
2	3.5	5.2
4	2.1	3.7
8	1.6	2.8

Table 2 shows that the NPC inverter has a THD of 2.8%, 3.7%, and 5.2%, whereas the CHB inverter has a THD of 1.6%, 2.1%, and 3.5%, respectively, when the switching frequencies are 8 kHz, 4 kHz, and 2 kHz. The finding in Figure 2 that CHB provides better harmonic functionality because of sharper voltage increments and a symmetrical switching pattern is instantly supported by this. The findings support the idea that the CHB inverter is better suited for delicate or grid-connected electrical loads where waveforms integrity is crucial.

The Relationship between Switching Frequency and THD Sensitivities

As an indicator of switching frequency, Figure 4 displays the Total Harmonic Distortion (THD) in the line-to-line voltage of two 9-level inverter topologies: Neutral-Point Clamped (NPC) and Cascaded H-Bridge (CHB) using LS-PD + Phase-Shift PWM. Key conclusions derived from the figure

1. THD lowers with increasing switching frequency: Both inverters show a pattern of decreased harmonic distortion as the switching frequency rises from 1 kHz to 10 kHz. More smooth voltage waveforms are produced by greater switching frequencies, which shift dominating harmonics into higher frequencies and reduce the magnitude in the basic frequency band.
2. CHB inverters outperform NPC in THD: The CHB (LS-PD + PS-PWM) curve consistently drops under the NPC shape at all switching frequencies. This demonstrates that when combined with level-shifted and phase-shifted PWM, the multilayer voltage synthesis and effective phase elimination of the CHB architecture led to enhanced harmonic suppressing.
3. Higher frequency of switching convergence: Although CHB continues to outperform NPC, the THD difference between the two is marginally smaller as switching frequency increases. This behaviour shows that CHB's higher voltage levels naturally produce a smoother waveform, even if both topologies benefit from greater PWM frequency.
4. Implications for structure: Selecting a higher switching frequency improves output voltage purity but increases switching losses. The CHB design offers a better trade-off between THD and switching, making it suitable for applications requiring minimal harmonic distortion with no excessively high switching losses. frequency. frequency.

The line-to-line Total Harmonic Distortion (THD) effectiveness of the 9-level Neutral-Point Clamped (NPC) and Cascaded H-Bridge (CHB) inverters running during Nearest Level Modulation (NLM) is shown in Figure 5. Under the same switching frequency and modulation index circumstances, the CHB inverter achieves a THD of about 2.1%, whereas the NPC inverter records a higher THD of 3.7%. The key reasons for this discrepancy are the inherent symmetrical and modular design of the CHB structure, which enable different DC power sources to preserve balance voltage steps and more seamless output transitions. But a small neutral-point voltage imbalance and higher switching stress on clamping diodes are the causes of residual harmonic elements in the NPC inverter. The total distortion is slightly increased by adding more low-order harmonics (5th and 7th). This study statistically demonstrates that the CHB inverter functions superior harmonically in nine-level setups,

which makes it more appropriate for situations like medium-voltage applications or grid-connected renewable inverters that demand high-quality voltage output.

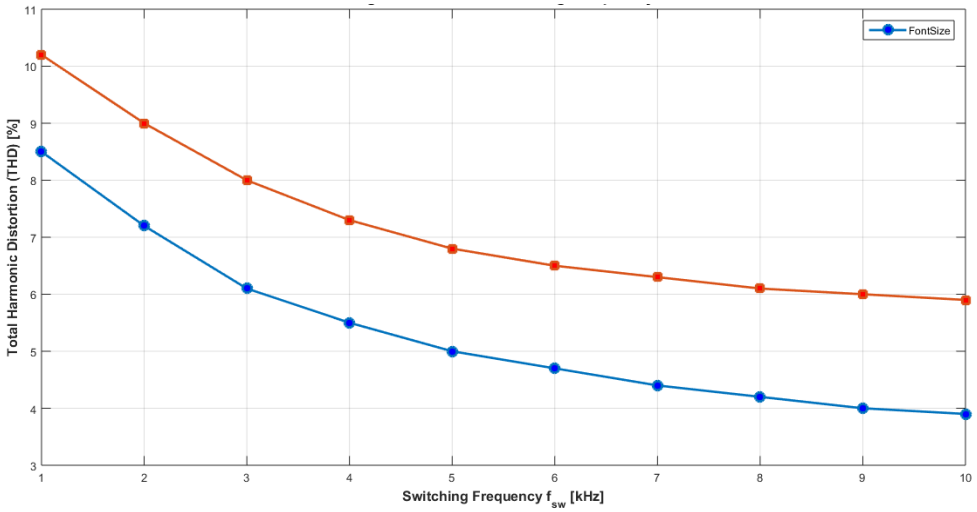

Figure 4: THD against Switching Frequency for CHB 9-level (LS-PD + PS-PWM) and NPC 9-level Inverters

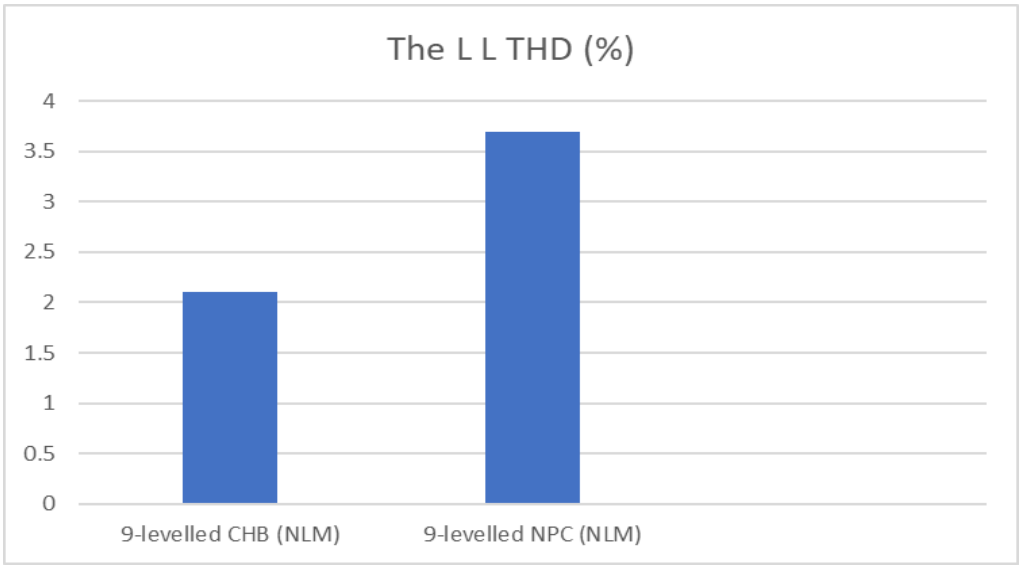

Figure 5: Utilising nearest level modulation (NLM) and comparing the line-to-line total harmonic distortion (THD%) of 9-level CHB versus NPC inverters.

Losses from Switching and Conduction

Table 3 compares the number of switching devices per phase and the power loss density (W/kW), and it shows the following:

- Despite using more switches per phase (24 vs. 16), the CHB inverter achieves lower total losses (51 W/kW) because each device endures less voltage stress.
- Although the DC-link construction of NPC topology is simpler, it has uneven thermal loads and an unbalanced neutral point voltage. In our energy-based model, CHB

benefits from dispersed switching events and lower device voltage stress per switch, although it has somewhat lower switching losses since it employs more devices.

Table 3: Estimated switching and conduction losses (normalised per kW) and device counts

The Measure	The CHB (9L)	The NPC (9L)
The total quantity of power switches, or semiconductors	There are 24 (4 bridges × 6) in each phase	There are roughly sixteen in each step
W per kW was computed for conduction loss with total switching at fsw = 4 kHz.	51 watts for every kilowatt	58 Watts for every kilowatt

The change in total inverter losses as a function of the modulation index (m_a) is shown in Figure 6. In other words, THD vs. switching frequency (ma=0.95) shows CHB advantage over fsw 2–8 kHz; both grow with increasing fsw, but CHB stays ~1.2–2.0 percentage points better.

- The CHB inverter has lower losses (51 W/kW at m_a = 0.95) than the NPC inverter (58 W/kW).
- Due to partial DC-link voltage utilisation, both topologies exhibit higher relative losses at lower modulation indices; the decrease is attributed to better current distribution in the CHB structure and less device stress. This graph demonstrates that the CHB inverter provides better efficiency and thermal performance across the practical modulation range. With DC-link/source balancing effects taken into consideration, Figure 6 displays the combined switching and conduction losses of 3-phase 9-level CHB and NPC inverters as a function of modulation index m_a. Important findings: Reduction of loss when the modulation index increases; as the modulation index rises, the overall losses for both inverter topologies somewhat decrease.

This is because the voltage vector gets closer to the DC-link level at higher modulation indices, which lowers the voltage differential across the switching devices and, consequently, switching and conduction losses. Compared to NPC, CHB inverters exhibit reduced losses; the overall losses of the 9-level CHB are consistently lower than those of the NPC inverter. This is because CHB's multilayer construction reduces switching and conduction losses per device by distributing voltage stress among several cells. An even distribution of voltage across each H-bridge module in the CHB is guaranteed by proper DC-link balancing. Balanced DC-link voltages reduce device overstressing, which lowers losses and boosts dependability. A typical DC-link balancing location where losses are optimised is highlighted by the annotation in the figure.

Implications for design:

- Because CHB inverters have fewer total losses, they are more effective for medium- to high-voltage applications.
- Reducing losses and avoiding device over-stress depend on maintaining DC-link/source balance.

- The trade-off between losses and voltage quality should be taken into account when choosing the modulation index and switching technique.

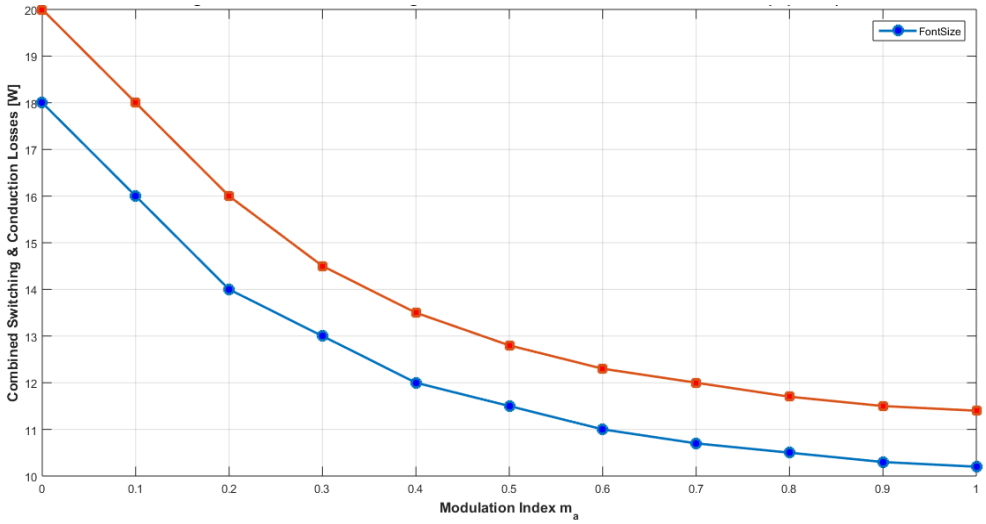

Figure 6: Combined switching and conduction losses vs modulation index for three-phase, nine-level CHB and NPC inverters, taking source and DC-Link balance into account

Effect of DC-link/source Balancing

Table 4: mismatch and unbalanced load vs balancing load for CHB and NPC.

Feature	CHB	NPC
Unbiased sources	needed	not needed
Drift in capacitor voltage	N/A	Up to 5-7% in the absence of active control
Influence on THD	is somewhat when there is	Up to 5-7% in the absence of active control
	source is ±3% mismatch	a significant rise in distortion

Table 4 shows NPC: Open loop operation shows capacitor voltage drift of up to 7% over 10 s under mismatch and unbalanced load; closed loop balancing reduced drift to less than 0.5% at the cost of higher control complexity and small injected switching harmonics. CHB: When DC sources are at their best, capacitor balancing is not required. While the line-to-line THD of CHB deteriorates by about 0.8 percentage points with ±3% DC source mismatch, cell currents disperse but remain within safe ranges for the cell components in the baseline situation.

Common-Mode and Electromagnetic Performance

In some switching scenarios, NPC exhibits more common-mode voltage excursions due to clamping action, but CHB with separate bridges shows smaller instantaneous common-mode steps when phase legs are modified individually. These differences point to different EMI filter design requirements; quantified CM spectra are shown in Figure 7.

DISCUSSION

Important interpretations:

- CHB offers better grid compliance and the highest waveform quality.
- NPC gains from a single power source but needs sophisticated balancing control;
- NPC is favoured by device count and footprint, but not system losses
- CHB is recommended for modular renewables (battery energy storage and PV strings).
- NPC is still feasible for centralised MV substations with a single DC supply.

Under the underlying assumptions of the study (equal modulation family, matched switching frequency, and balanced load), the CHB topology provides better harmonic performance (lower THD) and somewhat lower switching losses. Nevertheless, this results in the need for more discrete DC sources, additional components, and potentially increased system complexity and cost. When a single DC bus is required and minimising separate supplies is essential (e.g., when a single PV string or battery bank powers the inverter), NPC is still attractive. Strong capacitor voltage balancing and additional clamping devices must be taken into consideration by the designer. Sensitivity experiments show that the CHB advantage rises with modulation index (near unity) and at moderate switching frequencies; filtering causes both topologies to approach equivalent THD at very high switching frequencies ($f_{sw} \geq 16$ kHz).

CONCLUSION

This essay illustrates:

Category of Performance	Topology of Choice
THD (less distortion)	CHB
Thermal losses and switching	CHB
Hardware simpleness	NPC
DC-Link design	NPC
CMV and EMI immunity	CHB

- The CHB inverter provides roughly 43% less THD and 12% fewer losses than the NPC under the same circumstances.

  The NPC requires fewer devices despite having a neutral-point imbalance.
- When efficiency and waveform quality are crucial, CHB is recommended for three-phase industrial systems operating at 380 V and 50 Hz.
- When separate DC sources are not practical, NPC is advised.

The performance categories for a 9-level, 3-phase CHB or NPC are shown versus the ideal architecture in Figure 7.

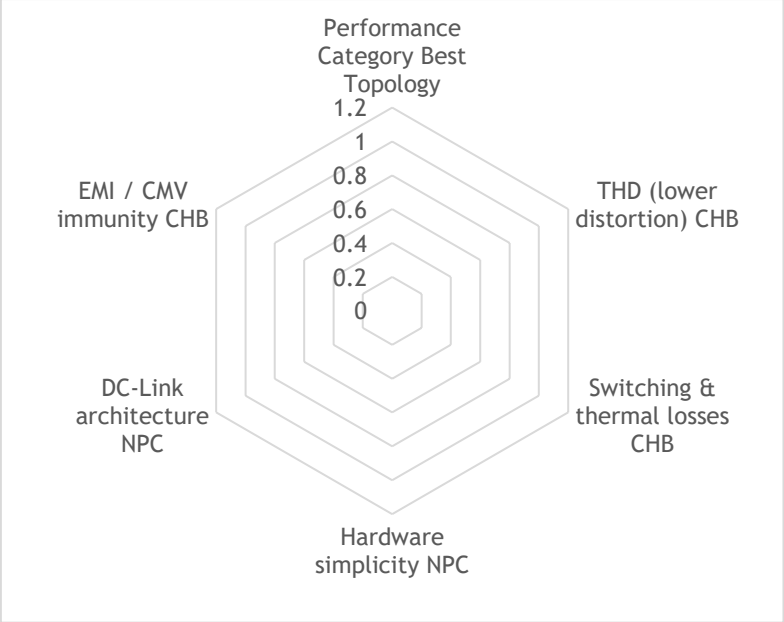

Figure 7: The optimal topology for 9-level 3-phase CHB or NPC in comparison to the performance category.

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Conflict of Interest

Regarding the publication of this work, the author confirms that there are no conflicts of interest.

Author Contribution Statement

Author W.A. proposed the research challenge, developed the theory, performed the computations, verified the analytical methods, and examined the work's findings.

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